

REMARKS/ARGUMENTS

Claims 7-21 were previously pending in the application. Claims 9, 13, 19 and 21 are canceled and new claims 22-24 are added. Therefore, claims 7, 8, 10-12, 14-18, 20 and 22-24 are presented for consideration.

Claims 7, 8, 12, 14, 15 and 17 are rejected as unpatentable over TAKIAR et al. 5,502,289 in view of MCCUTCHEON 5,552,209. This rejection is respectfully traversed.

Independent claim 7 is amended to recite a copper foil layer traversing a wiring layer from a first bonding pad on the wiring layer to a second bonding pad on the wiring layer, the copper foil layer is connected to a substrate only at the first bonding pad, and is connected to a second semiconductor chip only at the second bonding pad.

By way of example, Figure 2 of the present application shows the copper foil layer 72 traversing the wiring layer 7 from a first bonding pad 71b to a second bonding pad 71a. The copper foil layer 72 is connected to the substrate 1 only at the first bonding pad 71b and is connected to the second semiconductor chip 3 only at the second bonding pad 71a.

Each of the figures of TAKIAR et al. that show a connection between a wiring substrate and a second semiconductor chip show two bonding pads of the wiring layer connected to the

second semiconductor chip. In addition, none of the figures of TAKIAR et al. show a copper foil layer connected to the substrate at only a first bonding pad of the wiring layer as recited in claim 7 of the present application.

MCCUTCHEON is only cited for the teaching of a wiring layer having a polyimide tape and a copper foil layer therebetween. MCCUTCHEON does not teach or suggest that the copper foil layer traverses the wiring layer from a first bonding pad to a second bonding pad, that the copper foil layer is connected to the substrate through a first bonding wire only at the first bonding pad, and that the copper foil layer is connected to the second semiconductor chip through a second bonding wire only at the second bonding pad as recited in claim 7 of the present application.

The above noted features are missing from each of the references, are absent from the combination and thus are not obvious to one having ordinary skill in the art. Accordingly, reconsideration and allowance of claim 7 are respectfully requested. Claim 8 depends from claim 7 is also believed patentable over the cited prior art.

Independent claim 12 provides that the conductor inside the wiring layer is outside the second semiconductor chip and is connected to a first bonding pad on the wiring layer nearest a first edge of the second semiconductor chip and is connected to a

second bonding pad on the wiring layer nearest a second edge of the second semiconductor chip and that the conductor is connected to the substrate only at the first bonding pad, and the conductor is connected to the second semiconductor chip only at the second bonding pad.

By way of example, Figure 2 of the present application shows the conductor 72 inside the wiring layer 7 is outside the second semiconductor chip 3 and is connected to a first bonding pad 71b on the wiring layer 7 nearest a first edge of the second chip 3 and is connected to a second bonding pad 71a on the wiring layer 7 nearest a second edge of the second chip 3 and that the conductor 72 is connected to the substrate 1 only at the first bonding pad 71b, and the conductor is connected to the second semiconductor chip 3 only at the second bonding pad 71a.

As stated above, each of the figures of TAKIAR et al. that show a connection between a wiring substrate and a second semiconductor chip show two bonding pads of the wiring layer connected to the second semiconductor chip. In addition, none of the figures of TAKIAR et al. show a copper foil layer connected to the substrate at only a first bonding pad of the wiring layer as recited in claim 12 of the present application.

As also set forth above, MCCUTCHEON is only cited for the teaching of a wiring layer having a polyimide tape and a copper foil layer therebetween. MCCUTCHEON does not teach or

suggest what is recited in claim 12. Accordingly, reconsideration and withdrawal of the rejection are respectfully requested.

Claims 14 and 15 depend from claim 12 and are also believed patentable over the cited prior art.

Independent claim 17 recites that a conductor that traverses the wiring layer from a first bonding pad to a second bonding pad, is connected to the substrate only at the first bonding pad, and is connected to the second semiconductor chip only at the second bonding pad. The comments above regarding claim 7 are equally applicable to claim 17.

Claims 9, 13 and 19 are rejected as unpatentable over TAKIAR et al. in view of MCCUTCHEON and further in view of BEILSTEIN, Jr. et al. 5,567,654.

Claims 9, 13 and 19 are canceled and thus this rejection is believed moot.

Claims 10, 11, 16, 18 and 20 are rejected as unpatentable over TAKIAR et al. in view of MCCUTCHEON and further in view of TOKUDA et al. 5,870,289. This rejection is respectfully traversed.

TOKUDA et al. is only cited for the teaching of a via hole on the wiring layer connected to a bonding pad of a semiconductor chip. TOKUDA et al. do not disclose or suggest what is recited in claims 7, 12, 17 and 20. As noted above, TAKIAR et al. and MCCUTCHEON do not teach or suggest what is

recited in claims 7, 12 and 17. Since claims 10, 11, 16 and 18 depend from claims 7, 12 and 17 respectively, and further define the invention, the combination of references would not render obvious claims 10, 11, 16 and 18.

Claim 20 also provides that a copper foil layer is outside the second semiconductor chip and is connected to a first bonding pad on the wiring layer nearest a first edge of the second semiconductor chip and is connected to a second bonding pad on said wiring layer nearest a second edge of the second semiconductor chip and that the copper foil layer is connected to the substrate only at the first bonding pad, and is connected to the second semiconductor chip only at the second bonding pad. The comments above regarding claim 12 are equally applicable to claim 20 as to TAKIAR et al. in view of MCCUTCHEON. As noted above, TOKUDA et al. do not teach or suggest what is recited in claim 20. Accordingly, the combination of references would not render obvious claim 20.

Claim 21 is rejected as unpatentable over TAKIAR et al. in view of MCCUTCHEON and further in view of TOKUDA et al. and BEILSTEIN, Jr. et al.

Claim 21 is canceled rendering the above rejection moot.

New claims 22 and 23 provide that the second edge is opposite the first edge as seen in Figure 2, for example. New

claim 24 provides that the wiring layer is integral with the first semiconductor chip as seen in Figure 6 of the present application, for example. These features are not disclosed or suggested by the combination of references.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

Should there be any matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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